1. A dual-bit split gate flash memory comprising:

a plurality of memory cells wherein each memory cell comprises:

a select gate overlying a substrate and isolated from said substrate by a select gate oxide layer;

a first and second floating gate on opposite sidewalls of said select gate and isolated from said select gate by an oxide spacer; and

a control gate overlying said select gate and said first and second floating gates and isolated from said select gate and said first and second floating gates by a dielectric layer; and

source and drain regions within said substrate and shared by adjacent said memory cells.

2. The memory according to Claim 1 wherein a channel length under said select gate and said first and second floating gates is between about 0.05 and 0.07 microns in 0.18 micron technology.

3. The memory according to Claim 1 wherein said select gate comprises:

a polysilicon layer having a thickness of between about 1000 and 1200 Angstroms; and

a dielectric capping layer having a thickness of between about 800 and 1000 Angstroms.

4. The memory according to Claim 3 wherein said dielectric capping layer comprises high temperature oxide.

5. The memory according to Claim 1 wherein said select gate oxide has a thickness of between about 29 and 35 Angstroms.

6. The memory according to Claim 1 wherein said oxide spacer comprises high temperature oxide and has a width of between about 400 and 500 Angstroms.

7. The memory according to Claim 1 wherein first and second floating gates are isolated from said substrate by a tunneling oxide having a thickness of between about 80 and 100 Angstroms.

8. The memory according to Claim 1 wherein said first and second floating gates have a thickness of between about 1300 and 1600 Angstroms and a length of between about 500 and 700 Angstroms.

9. The memory according to Claim 1 wherein said control gate comprises polysilicon having a thickness of between about 2000 and 2400 Angstroms.

10. The memory according to Claim 1 wherein said dielectric layer comprises a first layer of high temperature oxide, a second layer of silicon nitride, and a third layer of high temperature oxide, each layer having a thickness of between about 60 and 70 Angstroms.

11. A method of fabricating a dual-bit split gate flash memory comprising:

providing a select gate oxide layer on the surface of a substrate;

depositing a first polysilicon layer overlying said select gate oxide layer;

depositing a capping layer overlying said first polysilicon layer;

patterning said capping layer, said first polysilicon layer and said select gate layer to form a plurality of select gates;

forming spacers on sidewalls of said select gates;

growing a tunneling oxide layer on said substrate exposed between said select gates;

depositing a second polysilicon layer overlying

said tunneling oxide layer and said select gates and etching back said second polysilicon layer to below a top surface of said select gates;

depositing an interpoly dielectric layer overlying said second polysilicon layer and said select gates;

depositing a third polysilicon layer overlying said interpoly dielectric layer;

depositing a capping oxide layer overlying said third polysilicon layer;

patterning said capping oxide layer, said third polysilicon layer, and said second polysilicon layer to form a plurality of memory cells wherein a portion of said second polysilicon layer remains on either side of each of said select gates forming first and second floating gates for each memory cell and wherein said third polysilicon layer covers said select gate and said first and second floating gate of each said memory cell and forms a control gate; and

implanting ions to form source and drain regions within said substrate between said memory cells wherein said source and drain regions are shared by adjacent memory cells to complete fabrication of said dual-bit split gate flash memory.

12. The method according to Claim 11 wherein said select gate oxide layer has a thickness of between about 29 and 30 Angstroms.

13. The method according to Claim 11 wherein said first polysilicon layer has a thickness of between about 1000 and 1200 Angstroms.

14. The method according to Claim 11 wherein said capping layer comprises high temperature oxide having a thickness of between about 800 and 1000 Angstroms.

15. The method according to Claim 11 wherein said spacers comprise high temperature oxide and have a width of between about 400 and 500 Angstroms.

16. The method according to Claim 11 wherein tunneling oxide has a thickness of between about 80 and 100 Angstroms.

17. The method according to Claim 11 wherein said step of depositing said interpoly dielectric layer comprises:

depositing a first high temperature oxide layer overlying said second polysilicon layer and said select gates;

depositing a silicon nitride layer overlying said first high temperature oxide layer; and

depositing a second high temperature oxide layer overlying said silicon nitride layer wherein each of said layers has a thickness of between about 60 and 70 Angstroms.

18. The method according to Claim 11 wherein third polysilicon layer has a thickness of between about 2000 and 2400 Angstroms.

19. The method according to Claim 11 wherein said capping oxide layer comprises TEOS oxide having a thickness of between about 1000 and 1300 Angstroms.

20. A method of programming a dual-bit split gate flash memory comprising:

providing a plurality of memory cells wherein each memory cell comprises:

a select gate overlying a substrate and isolated from said substrate by a select gate oxide layer;

a first and second floating gate on opposite sidewalls of said select gate and isolated from said select gate by an oxide spacer; and

a control gate overlying said select gate and said first and second floating gates and isolated from said select gate and said first and second floating gates by a dielectric layer; and

providing source and drain regions within said substrate and shared by adjacent said memory cells;

wherein said first floating gate of a memory cell adjacent to said drain is to be programed, said programming method comprising:

applying a positive select gate voltage to said select gate of said memory cell;

applying a positive control gate voltage to said control gate of said memory cell;

applying a positive drain voltage to said drain and connecting said source to ground; and

connecting said substrate to ground wherein hot electrons are injected from said source to said drain and into said first floating gate to program said first floating gate of said memory cell.

21. A method of programming a dual-bit split gate flash memory comprising:

providing a plurality of memory cells wherein each memory cell comprises:

a select gate overlying a substrate and

isolated from said substrate by a select gate oxide layer;

a first and second floating gate on opposite sidewalls of said select gate and isolated from said select gate by an oxide spacer; and

a control gate overlying said select gate and said first and second floating gates and isolated from said select gate and said first and second floating gates by a dielectric layer; and

providing source and drain regions within said substrate and shared by adjacent said memory cells;

wherein said second floating gate of a memory cell adjacent to said source is to be programed, said programming method comprising:

applying a positive select gate voltage to said select gate of said memory cell;

applying a positive control gate voltage to said control gate of said memory cell;

applying a positive source voltage to said source and connecting said drain to ground; and

connecting said substrate to ground wherein hot electrons are injected from said drain to said source and into said second floating gate to program said second floating gate of said memory cell.

22. A method of erasing a dual-bit split gate flash memory comprising:

providing a plurality of memory cells wherein each memory cell comprises:

a select gate overlying a substrate and isolated from said substrate by a select gate oxide layer;

a first and second floating gate on opposite sidewalls of said select gate and isolated from said select gate by an oxide spacer; and

a control gate overlying said select gate and said first and second floating gates and isolated from said select gate and said first and second floating gates by a dielectric layer; and

providing source and drain regions within said substrate and shared by adjacent said memory cells;

wherein said first floating gate of a memory cell adjacent to said drain is to be erased, said erasing method comprising:

applying a negative control gate voltage to said control gate of said memory cell;

applying a positive drain voltage to said drain and connecting said source to ground; and

connecting said substrate to ground wherein electrons are tunneled from said first floating gate

into said drain to erase said first floating gate of said memory cell.

23. A method of erasing a dual-bit split gate flash memory comprising:

providing a plurality of memory cells wherein each memory cell comprises:

a select gate overlying a substrate and isolated from said substrate by a select gate oxide layer;

a first and second floating gate on opposite sidewalls of said select gate and isolated from said select gate by an oxide spacer; and

a control gate overlying said select gate and said first and second floating gates and isolated from said select gate and said first and second floating gates by a dielectric layer; and

providing source and drain regions within said substrate and shared by adjacent said memory cells;

wherein said second floating gate of a memory cell adjacent to said source is to be erased, said erasing method comprising:

applying a negative control gate voltage to said control gate of said memory cell;

applying a positive source voltage to said

source and connecting said drain to ground; and

connecting said substrate to ground wherein electrons are tunneled from said second floating gate into said source to erase said second floating gate of said memory cell.

24. A method of reading a dual-bit split gate flash memory comprising:

providing a plurality of memory cells wherein each memory cell comprises:

a select gate overlying a substrate and isolated from said substrate by a select gate oxide layer;

a first and second floating gate on opposite sidewalls of said select gate and isolated from said select gate by an oxide spacer; and

a control gate overlying said select gate and said first and second floating gates and isolated from said select gate and said first and second floating gates by a dielectric layer; and

providing source and drain regions within said substrate and shared by adjacent said memory cells;

wherein said first floating gate of a memory cell adjacent to said drain is to be read, said reading method comprising:

applying a positive select gate voltage to said select gate of said memory cell;

applying a positive control gate voltage to said control gate of said memory cell;

applying a positive source voltage to said source;

applying a zero drain voltage to said drain; and

connecting said substrate to ground wherein a channel under said second floating gate is forced into conductive depletion to read said first floating gate of said memory cell.

25. A method of reading a dual-bit split gate flash memory comprising:

providing a plurality of memory cells wherein each memory cell comprises:

a select gate overlying a substrate and isolated from said substrate by a select gate oxide layer;

a first and second floating gate on opposite sidewalls of said select gate and isolated from said select gate by an oxide spacer; and

a control gate overlying said select gate and said first and second floating gates and isolated from

said select gate and said first and second floating gates by a dielectric layer; and

providing source and drain regions within said substrate and shared by adjacent said memory cells;

wherein said second floating gate of a memory cell adjacent to said source is to be read, said reading method comprising:

applying a positive select gate voltage to said select gate of said memory cell;

applying a positive control gate voltage to said control gate of said memory cell;

applying a positive drain voltage to said drain;

applying a zero source voltage to said source; and

connecting said substrate to ground wherein a channel under said first floating gate is forced into conductive depletion to read said second floating gate of said memory cell.